ELECTRONIC DEVICES BASED ON 2D MATERIAL: FABRICATION, CHARACTERIZATION AND ANALYSIS

BY

JIALUN LIU

THESIS

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Adviser:

Assistant Professor Wenjuan Zhu

Abstract

Two-dimensional (2D) crystals are layered materials with strong in-plane covalent bonding and weak Van der Waals interlayer coupling. Stable 2D materials range from insulators, to semiconductors, to metals and even superconductors. Compared to their bulk counterparts, 2D materials show many inherent unique properties in their atomically thin layers, such as high flexibility, high surface-to-bulk ratio and absence of surface dangling bonds. These distinctive properties make 2D materials promising in many applications, including logic gates, flexible electronics, communication and biomedical sensing. A successful pathway to develop these materials into mature future devices relies on characterization of their electronic properties and incorporating them with other materials.

In this thesis, we studied the intrinsic and extrinsic properties of black phosphorus (BP) by AC conductance and capacitance methods. Black phosphorus capacitors with various types of gate dielectrics were fabricated and measured at varying temperatures. From the temperature dependence of the transition frequency, we determined the bandgap of the ~50 nm black phosphorus is 0.31 eV, while, from electrostatic models, our simulated bandgap is ~0.37 eV and doping is ~3×10^{18} $cm^{-}3$. From the AC conductance of the BP/Al_2O_3 and BP/boron nitride (BN) capacitors, we extracted the interface trap density and time constant and found that the interface trap density in Al_2O_3 is about 10 times that in BP/BN capacitors, indicating the superior quality of the single-crystal BN. We confirmed that the interface trap density increases and the time constant decreases as the trap level approaches the valence band. We also found that BP is naturally p-type doped, and the doping concentration in BP/BN capacitors is much higher than that in BP/Al_2O_3 capacitors. This may be due to the fact that the Al_2O_3 deposited by ALD introduces n-type doping in the black phosphorus. These characterization techniques along with the intrinsic and extrinsic properties of the black phosphors obtained in this study will be very important for designing and optimizing electronic devices (such as metal-oxide field effect transistors, tunneling field effect transistor, and resonant tunneling diodes) based on BP.

Acknowledgments

Firstly, I would like to deliver my most sincere gratitude to my graduate research adviser, Prof. Wenjuan Zhu, for letting me join her research group to pursue my master's degree. Her tireless guidance and encouragement have undoubtedly been the greatest support to my academic life in the University of Illinois. I also appreciate the help from our staff in MNTL, for building a wonderful work environment where we can fully engage in our research.

I would also like to thank the ECE department advising and editorial service for their professional advice and service during my completion of this work. Finally, thanks to my family and friends for their love and support.

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1. Introduction

The art of field-effect semiconductor devices is to use the electric field as a "switch" to control the current's on/off state. Following Moore's law,[1] since the 1960s the semiconductor industry has been scaling down semiconductor devices and lowering their cost while improving the electrical performance and enlarging the IC's density. Various structural/material innovations (SOI, FINFET, high-K gate dielectrics, strained silicon, etc.) and lithography techniques (DUV/EUV, immersion lithography, double patterning, etc.) have been invented and they successfully maintain this trend of scaling down semiconductors. From 1971 to 2014, the typical semiconductor manufacturing process was driven from 10μm to 14nm node for metal-oxide-semiconductor field-effect transistors (MOSFETs),[2] the building blocks for most of today's consumer electronics. Nevertheless, a further device miniaturization/speed-up is exceptionally challenging given nanoscale physical limitations and high development cost. Specifically, shrunken channel length with higher doping undermines the control of the top gate of the channel over the source/drain.[3] Typically these short-channel effects (SCEs) lead to drain-induced barrier lowering (DIBL), carrier surface scattering, hot electron effects and other undesired side-effects.[4] Electron mobility in silicon, severely degraded by surface roughness, is also inevitably affected by heavy doping in short-channel cases. Innovations in materials and structures are required to extend Moore's law, as many have suggested.

After graphene as an atomic layer was discovered, transistors made from it showed extraordinary mobility among other merits.[5] Although graphene's zero semi-metallic behavior brings about low switchability for transistors, this group of materials is recognized as important for potential applications in novel devices. For this reason, graphene and other 2D materials developed later with similar structure have aroused interest. In addition to digital logic devices, 2D materials with high surface-to-bulk ratio are naturally ideal for sensors with high sensitivity (e.g. biomedical sensors,

piezoelectric sensors). Their sheet-like property suggests their suitability in flexible electronic applications beyond organic flexible electronics.[6] 2D materials are a relatively new and rapidly growing field of study, with new material findings and device breakthroughs emerging rapidly. Still, issues like large-scale production and doping remain challenging in the exploration.

In the following chapter, a few kinds of important 2D materials studied in this area recently are briefly introduced. Their synthesis or growth methods are discussed. We will summarize the procedures to fabricate 2D material-based electronic devices, which are very different from those for traditional semiconductor devices. This process may include material yielding (CVD growth or mechanical exfoliation), identification, and transfer (bulk mass transfer or target transfer), along with other regular semiconductor device fabrication techniques (lithography, metal deposition and/or dielectric growth).

These fabrication techniques are applied to build our black phosphorus-based field-effect transistors and capacitors. For FETs, we followed previous reported work and produced back-gated FETs and we discuss the channel mobility extracted. For capacitors, hexagonal boron nitride and aluminum oxide are used as dielectrics and the data we extracted from multi-frequency C-V measurements indicates reasonable band gap, doping, and interface trap density. The temperature dependence of the capacitance also agrees with the model proposed.

In the last chapter, the limitations of our devices' performance and fabrication procedure are discussed and future directions for improvements are identified. 2D materials are a relatively new but active area at the intersection of multiple fields and we hope our work will lead to new findings for this material family.

2. Typical 2D Materials in Study

Since the appearance of single-layered graphene transistors, more members of the 2D material family have been found. Since our main research interest is electronic devices, in this chapter several kinds of 2D materials of interest are briefly reviewed.

2.1 Graphene

Graphene was the very first two-dimensional atomic crystal discovered[5] and its 2D structure[7] (shown in Figure 1[8]) gives it properties very different from those of other allotropes of carbon (graphite, Fullerene, carbon nanotube, etc.). Its advantages include superior mechanical strength, high electronic and thermal conductivity, and impermeability to gases, which attracts a lot of attention for potential applications. Since researchers successfully exfoliated single-layer graphene from its bulk counterpart (graphite) with its main contributor winning the Nobel Prize later in 2010, its enticing electrical properties have encouraged extensive research into making electronic devices beyond the current complementary metal oxide semiconductor (CMOS) technology. Graphene, a semi-metallic carbon layer with one atom thickness, has superior carrier density and mobility ~10,000 $\mathrm{cm}^2/(\mathrm{V}\cdot s)$ and therefore is promising for lower energy dissipation and faster operating speed in electronics. Unfortunately, besides large-scale growth issues, the inherent gapless nature in graphene restricts the energy states variety and brings about great challenges for people to switch graphene on/off for digital device applications.[6] Cutting graphene into nanoribbons or depositing graphene onto certain substrates is done to show the structure change, hence non-zero bandgap, in graphene. But these changes are overall insignificant and damage graphene's appealing carrier transport properties, or turn out to need further investigation.[9-12]

Despite this drawback for digital applications, graphene shows exciting prospects for conductive coating for flexible electronics due to its transparency, flexibility, low sheet resistance and high transmittance, provided contact resistance issues can be appropriately addressed. In addition, graphene-based transistors have proved promising for RF devices with high cut-off frequencies.[13] On the other hand, graphene's transparency in one or a few layers and its wavelength-independent absorption rate in a large range of light spectra make it a suitable candidate for a number of photonic devices. These include photodetectors, various kinds of laser devices, and optical modulators.[6]

As an important factor to be considered for industrial products incorporation, production methods (Figure 2[6]) for large-scale and uniform graphene are great challenges in current development. For research purposes, mechanical exfoliation from bulk graphite is used a lot for graphene and other 2D materials for its convenience and high-quality flakes. An alternative common way to yield graphene is to grow it on copper or nickel with a mixture of methane and hydrogen at as high as 1000 ˚C.[14, 15] Another method includes precipitation of graphene layer on SiC wafer but is very costly.[16]

It is worth noting that the whole methodology to develop graphene devices, from material synthesis, to characterization, to device fabrication, to measurements and analysis, is instructive and hence provides valuable references and guidance for the study and development of other 2D materials.

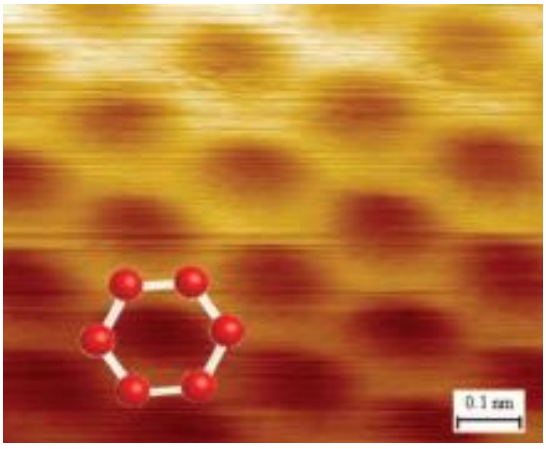


Figure 1: Graphene's honeycomb structure.

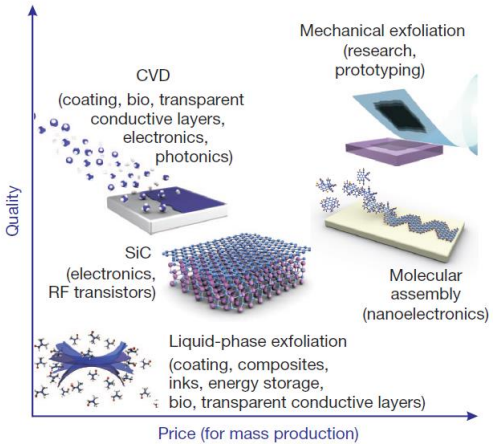


Figure 2: Several methods for mass production of graphene.

2.2 2D Transition Metal Dichalcogenides

Two-dimensional transition metal dichalcogenides (TMDC) have chemical formula MX_2 with transition element M and chalcogen X.[17] Among this group of materials MoS_2, WS_2, and WSe_2 have been studied in recent years for their high quality and stability in the isolation process. Like graphene, these materials can be readily exfoliated into one or a few layers by breaking the interlayer weak Van der Waals force without damaging intralayer covalent bonds (mechanical cleavage), or they can be grown by chemical vaporization deposition (CVD). As a representative example, a large area of atomic layer MoS_2 is often synthesized on a silicon wafer by CVD using MoO_3 and S powder with the help of PTAS as seeding material for nucleation. Figure 3[17, 18] demonstrates the structure of MoS_2 layers.

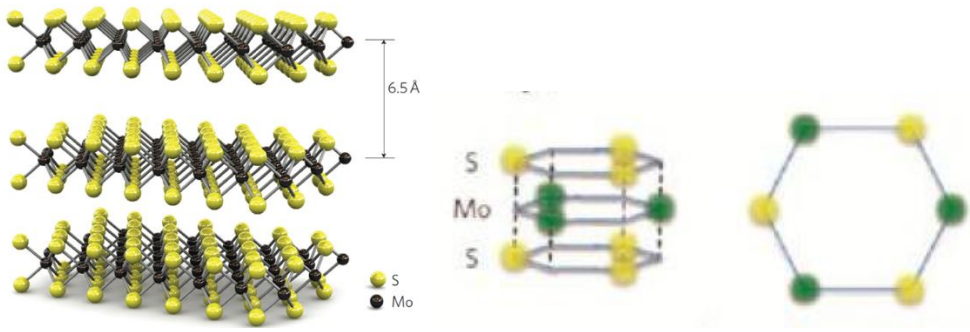


Figure 3: Honeycomb MoS_2 structures with alternating Mo and S atoms.

As the thickness decreases to a single layer, the band structure of TMDCs is changed by quantum confinement effects. A transition from indirect band gap (1.2 eV) at Γ point to direct band gap (1.9 eV) at K-point in the Brillouin zone is predicted and confirmed for MoS_2. This suggests its appealing properties in possible logic devices and optoelectronics. In fact, a top-gated single-layer MoS_2 FET was successfully fabricated in 2011 with appreciable mobility (~70 $cm^2/(V \cdot s)$), large on/off current ratio (~10^8) and satisfactory subthreshold swings (~74 mV/decade) at room temperature (Figure 4).[18] This device is demonstrated in Figure 4. After that, deeper investigation was carried out to understand the impact on carrier mobility of environmental gate dielectrics and the channel layer number. Also, despite

the inherent p or n type body by impurity charges, progress towards doping the TMDCs in a controllable way was made by several groups utilizing chemical treatment during/after crystal growth, for electronics fabrication with reliability and repeatability.[19]

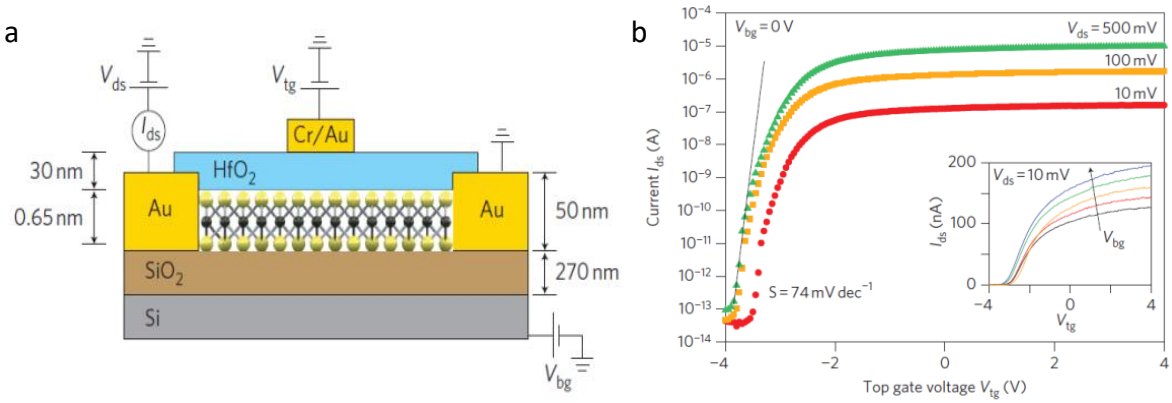


Figure 4: SL MoS_2 top-gated FET by B. Radisavljevic et al. (a) Device structure. (b) I-V characteristics.

The various band gap range of the TMDC family and its layer structure free of surface dangling bonds also provide exciting possibilities for applications based on epitaxy and heterostructure/junctions. The various direct band gap values and tunable features with layer numbers in visible light range also make TMDC optoelectronics attractive.[20] A phototransistor was made by single layer (SL) MoS_2 to show its potential as a photodetector with photo responsivity of 880 A/W at 561 nm wavelength light.[21] Finally, due to TMDC's M-X composition, the piezoelectric effect was examined in SL MoS_2 thin films, with the finding that no net piezoelectric effect is present within even number of layers or bulk counterparts due to the opposite orientation of alternating layers.[22]

2.3 Black Phosphorus

Compared to its allotropes (yellow/red/fibrous phosphorus), black phosphorus is most dense

and least reactive due to its interlinked six-membered ring. This unique puckered hexagonal structure (as shown in Figure 5) leads to anisotropic in-plane electrical and optical properties, which may offer special benefits in novel fields such as plasmonic devices.[23] Bulk black phosphorus has a direct band gap around 0.3 eV, while single layer black phosphorus is predicted to have a much larger band gap from 1 eV to 2 eV, depending on the theory model. This large variation indicates black phosphorus might be an ideal candidate for purposes requiring tunable band gap. Another notable point is this band gap range corresponds to the infrared range in the optical spectrum. Combined with other 2D materials' optical range from the band gap, heterostructures could be made for optoelectronics like high-efficiency solar cells. Black phosphorus used in devices is usually exfoliated from bulk crystal which could be made from red phosphorus under high temperature and/or high pressure although some innovative methods (including CVD) also exist.[24-26]

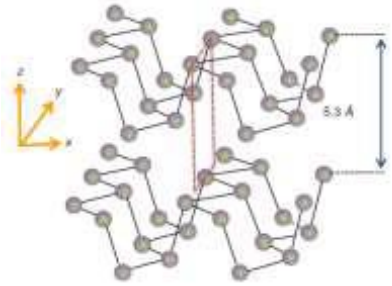


Figure 5: Puckered sheets of linked phosphorus atoms. Layer-to-layer space is ~0.5nm.

Back-gated FETs were fabricated by several independent groups.[23, 27, 28] In Figure 6, experimental data from the Zhang group[28] shows that a P-type FET device with 5nm thick BP channel is fabricated with 200 $\mathrm{cm}^2/(\mathrm{V}\cdot s)$ mobility with good on/off ratio at 10^5. As a comparison, the data here suggests the black phosphorus FET has higher mobility than that of a typical TMDC transistor while having a moderate (lower) on/off ratio.

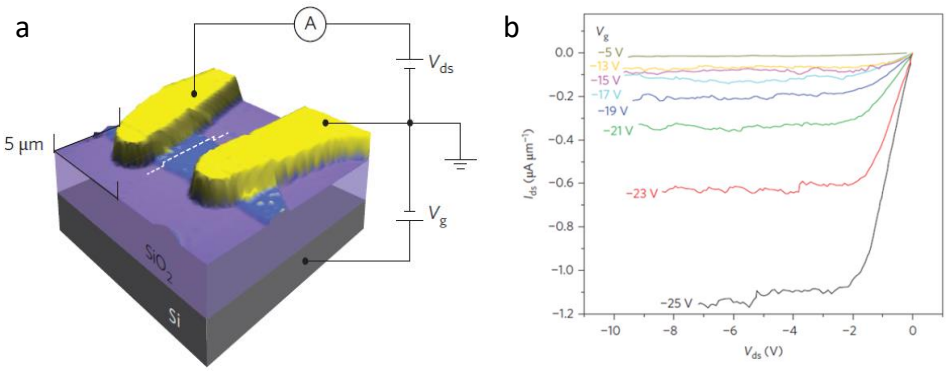


Figure 6: (a) A BP back gated transistor. (B) I_d-V_d curves under different gate bias.

However, instability might be an issue for making black phosphorus thin film devices since a few layers of black phosphorus gradually react with water and oxygen (as shown in Figure 7). Some recent experiments have assessed its surface reaction with the ambient environment and further work is expected to reveal this aspect of the material.[29]

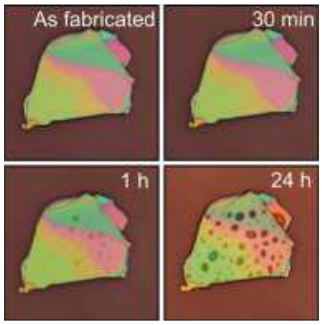


Figure 7: Optical images for mechanically exfoliated black phosphorus as time elapses.

2.4 Hexagonal Boron Nitride

Hexagonal boron nitride (hBN) is a III-V compound insulator with wide indirect bandgap around 6 eV.[30] It has a similar honeycomb structure to graphene except it is composed of alternating boron and

nitrogen atoms. hBN also has good mechanical strength and thermal/chemical stability. More importantly, it is experimentally suggested that graphene and other 2D semiconductors demonstrate remarkable mobility with hBN compared to other dielectrics due to their flat and low-impurity surfaces.[31] For these reasons, hBN is widely used as dielectric material or physical protection coating in 2D material transistors and heterostructures.[32-35]

The first CVD growth of monolayer hBN was developed by Kong's group in 2012,[36] using ammonia borane as precursor under LPCVD on copper foil. Other CVD growth methods for hBN also exist using precursors such as borazine.[37] Figure 8 consists of an AFM image of hBN[32] and a graphene-hBN transistor device demonstration.[33]

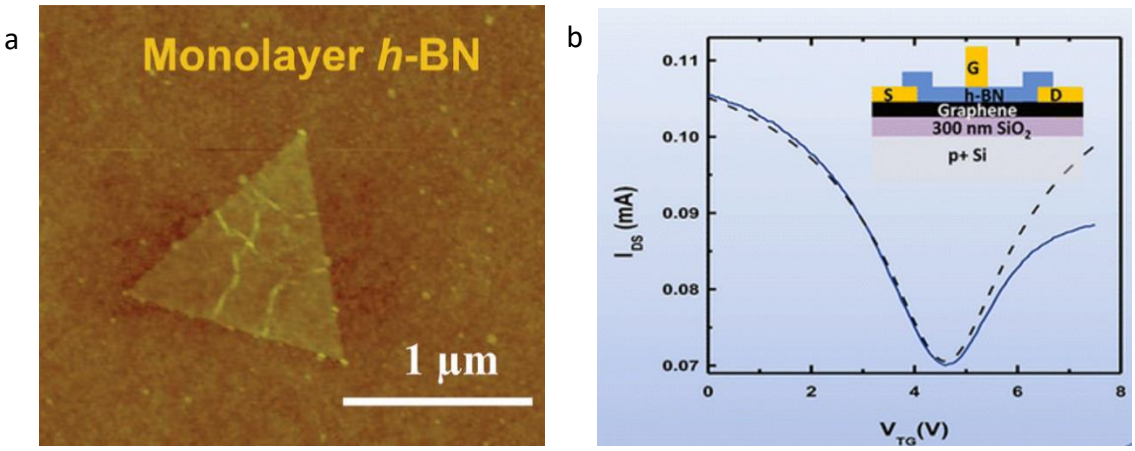


Figure 8: (a) CVD-grown hBN under AFM by Kim and (b) graphene transistor with hBN as dielectric.

3. Characterization/Fabrication Techniques for 2D Material Devices

Compared to mature III-V material, Ge or Si growth techniques used in wafer-scale substrates, 2D material used in electronic devices for research nowadays is usually cleaved from bulk crystal (mechanical transfer) or taken as a membrane from corresponding CVD substrate (wet transfer). In general, mechanically transferred 2D material flakes are relatively intact but their shapes and thickness are more random and uncontrollable due to the irreproducible process while splitting the bulk material into fragmented pieces. Sizes of these 2D material flakes are hence typically small. On the other hand, CVD-grown material provides the possibility for a larger (even wafer-scale) area of continuous material and the thickness of the flakes is more consistent through growth parameters (growth seeds, gas flow, temperature, time, etc.). But the material is likely to suffer from quality issues from the growth process and following transfer process with chemical etchant involved. Typically, for both material sources, they need to be transferred (from either bulk material or growth substrate) to dielectric substrates (SiO_2, quartz) to be further utilized in devices.

3.1 Mechanical Transfer – Exfoliation and Mass Printing

The method to yield "Scotch-tape graphene" used in the very first graphene transistor is widely known and forms the basis for the mechanical transfer method. For mass printing, magic tape or thermal-release tape is commonly used in labs. The following process includes typical steps for mechanical cleavage and transfer of 2D material from bulk crystal onto SiO_2 wafer or other substrates (adapted from manual provided by the 2D Semiconductors company).[38]

3.1.1 Preparation of Transfer Substrates

In general, a wafer with 90 nm or around 280~300 nm SiO_2 thickness is preferred for visible contrast between substrate and transferred 2D material flakes.[39] Acetone/IPA cleaning followed by N_2 air gun blow-dry is often applied, preferably with sonication treatment. In many cases, Piranha solution (sulfuric acid to 30% hydrogen peroxide with 3:1 ratio in volume) cleaning and oxygen plasma etching are also applied to clean the wafer and promote adhesion between flakes and substrate.[40] The process should be finished within ~1 hour after substrate pre-treatment for enhanced transfer rate.

In some special applications, quartz wafer or flexible polyimide substrates may be used to eliminate potential parasitic effects, depending on the device specification and requirements.

3.1.2 Transfer Process

1. Take a piece of 2D material crystal (a 1mm × 1mm area flake should suffice in most cases) and place it gently on a piece of Scotch-tape/thermal release tape (adhesive side). We will refer to this piece of tape as tape #1. This whole series of steps should be done with gloves on to minimized potential contamination. Tapes used in our lab are shown in Figure 9.

Figure 9: Magic tape/Scotch tape (top) and thermal release tape (bottom) often used in lab for mechanical transfer.

2. Prepare another piece of tape (tape #2) and lay it smoothly on tape #1 to enclose the crystal piece in both tapes. Let the tapes adhere completely and uniformly.
3. Split the tapes slowly from each other to exfoliate the flakes in the middle, as explained in Figure 10.[38] During the exfoliation, maintain steady and slow speed (<1 mm per second). A small angle should be kept between the two tapes during the process and tension should be applied along the tape. Tape #1 and tape #2 can then be saved as "mother tape".

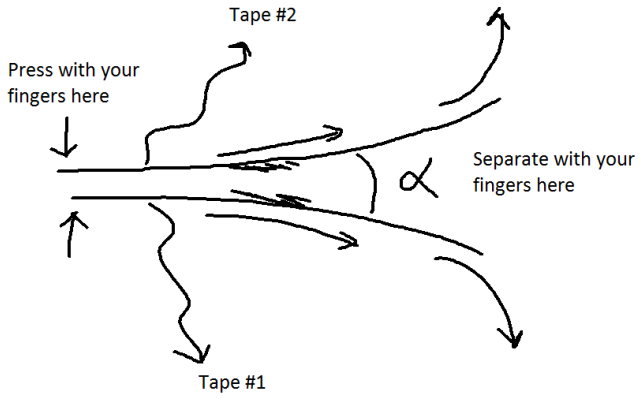


Figure 10: Splitting process demonstration.

4. Now take tape #3, adhere it to tape #2 and then split them, using same method described in step 2 and 3. Repeat this process a several times to split the original crystal into thinner parts. Note that these tapes could be saved in a sealed container for later use. (One could also simply fold and split the tape to thin down crystals with the cost of wasting part of the crystal.)
5. After crystals become sufficiently thin and cover a moderate area of the tape after several times of splitting, use the last tape (with thinnest flakes) and print it gently on the prepared substrate. Apply tension along the tape to make the contact between substrate and tape flat and uniform. Press gently to ensure sufficient contact.

6. Peel the tape away from the substrate after ~30 s of contact. Similar to the “tape duplication” process described in 2.3, exfoliation speed should still be slow (~0.5 mm/sec) and tension should be exerted along the tape as well. Keep in mind that a small angle between tape and substrate is important to a high yield of thin flakes on the target substrate. If thermal release tape is used, place the substrate with tape on a hot plate, a typical ~120 °C temperature will heat up the thermal release tape and it will curl up and separate from the substrate.

Since the crystal shape is random at the beginning and the exfoliation process is arbitrary, it is very hard to precisely control the size and shape of the resulting 2D material flake. However, this method and many other recipes tend to yield atomically thin flakes of interest among thick crystal fragment. In order to better understand the unique two-dimensional properties of the material, various inspection techniques are required to locate appropriate flakes (for characterization or device fabrication) on the substrate. Since many flakes of varying size, thickness and shape are distributed on the substrate at the same time and we need to inspect the whole area in search of a target flake of interest (usually one or a few layers), this is an example of a bottom-up procedure.

3.2 Mechanical Transfer – Exfoliation and Targeting Transfer

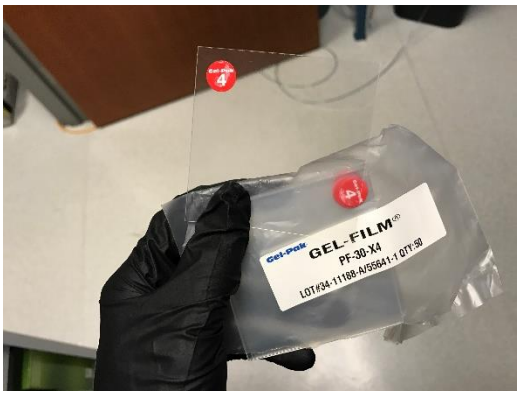
In many cases, we need our 2D material flake to be at a specific location on the substrate. For example, if a heterostructure stacking different 2D material flakes is proposed, we need to transfer the second layer of material exactly on the first target flake layer. While the first layer of material could be mass printed on the substrate using the method described in section 3.1, a targeting transfer is required to place the second layer on top of the first layer.

The key to accomplish such a goal is an appropriate transfer medium (usually some sacrificial adhesive solid/liquid chemical compound) which picks up the 2D material flakes from the tape or growth substrate. Then with help of the mechanical stage or system alike, the medium (with flakes) could be moved precisely and printed onto the target transfer area. Microscopes are often used to ensure accurate alignment before the contact between flakes on the medium and the target area on the substrate. The medium is then removed, leaving the transferred flake on the substrate.

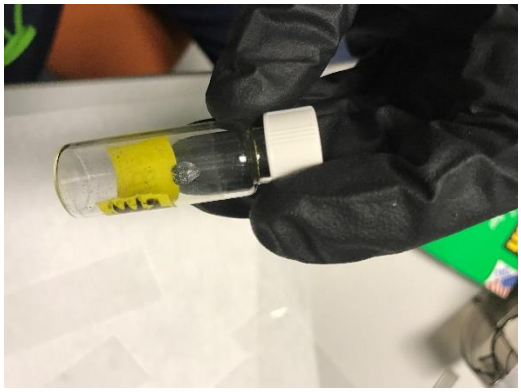
In the past, the wedging method, polyvinylalcohol (PVA) method and Evalcite method have been used to place 2D material flakes on the target position.[31, 41, 42] The wedging method uses water as the transfer-active agent to lift off the spin-coated hydrophobic polymer layer on hydrophilic substrate. If 2D material flakes on the hydrophilic surface are partially taken away by the hydrophobic layer, they can then be transferred elsewhere. The sacrificial layer needs to be removed by solvent after transfer. In the PVA method, flakes are transferred onto polymer sacrificial layer from substrate after the water soluble PVA polymer layer is dissolved in water. The sacrificial layer is then scooped up and mounted onto the manipulator for transfer. It also needs to be removed after transfer is done. The Evalcite method makes use of low glass temperature polymer, which is applied between the glass slide and picked-up flakes. After flakes on the glass slide are moved to the desired location, heat is applied and the polymer melts, leaving flakes to drop easily on the acceptor substrate. In all these methods, chemicals from the sacrificial layer are involved and might degrade the crystal quality and give a rise to capillary force.

Compared to these wet transfer methods, dry transfer methods use solidated viscoelastic material as the transfer medium (“stamp”) to carry the 2D material flakes without sacrificial layer dissolutions and they are low-cost, efficient and wet-chemical-free. Most dry transfer stamps are made of elastomer-based materials (polydimethylsiloxane, or PDMS, for example). In the series of photos in Figure 11, we briefly introduce the dry transfer tool based on *Gelfilm* (a polysiloxane based material

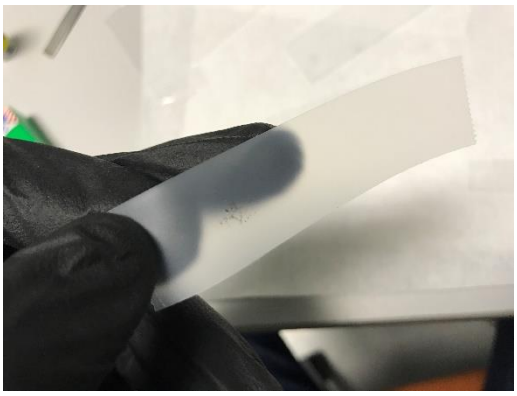
similar to PDMS film) and procedures used in our lab (adapted from the Castellanos-Gomez group's work[43]).



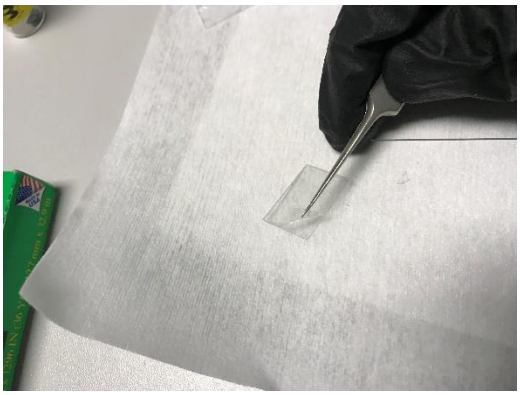
a. Prepare viscoelastic stamp (*Gelfilm* from *Gelkpak*).



b. Take a small piece out from the bulk material. (BP is shown here).

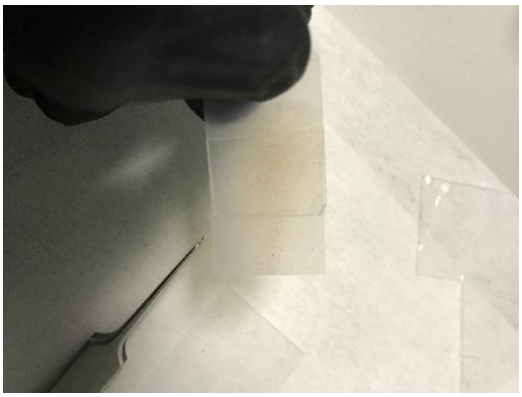


c. Smear the piece of crystal on Scotch-tape (see method described in 3.1).

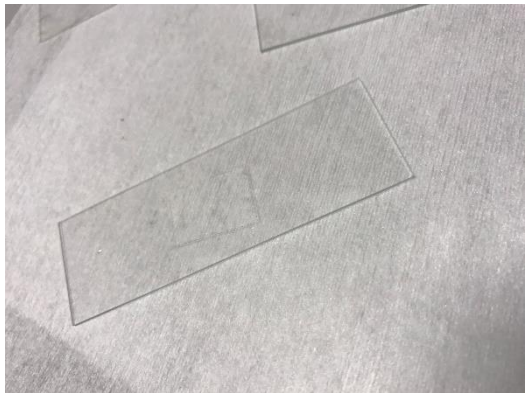


d. Print the tape with 2D material on cut-out Gelfilm (see method described in 3.1).

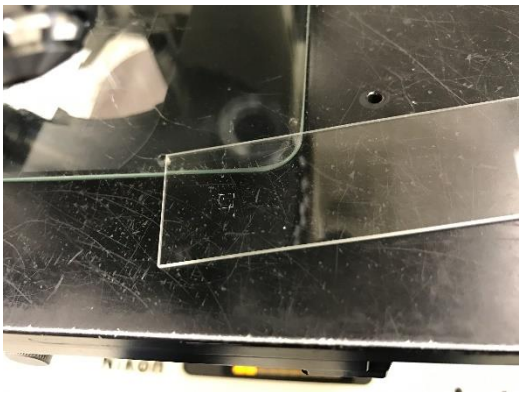
Figure 11: Procedures prior to target area contact.



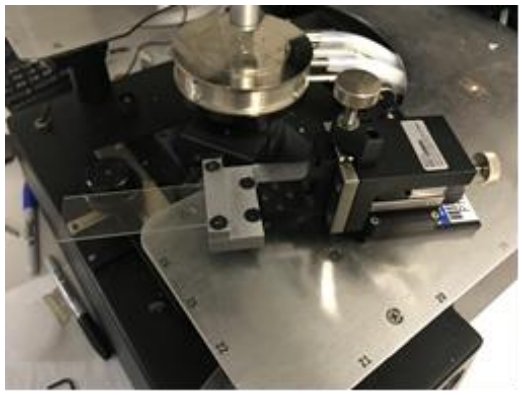
e. Peel the scotch tape with appropriate angle and speed after sufficient contact (see method described in 3.1).



f. Inspect the 2D material flakes yielded on *Gelfilm* (refer to 3.4) under optical microscope and locate the appropriate target area of interest.



g. Cut out the area of interest and place the *Gelfilm* on glass slide. In this way flakes are easier to track with later under microscope prior to contact.



h. Mount the glass slide on micromanipulator and place acceptor substrate (SiO_2) on object stage. With the mechanical arm, align the *Gelfilm* on top to start aligning.

Figure 11: Continued.

After the *Gelfilm* is brought into proximity with the substrate, use low amplification and xy adjustment of the manipulator to roughly align the target flake on the *Gelfilm* with the target area on the substrate. The focus of the microscope may need to switch between film and substrate due to different heights. Lower the glass slide with the z direction of the manipulator. Use high amplification for fine alignment right before the contact of the two surfaces. Focus on the substrate and observe the

overlapping of target flake and target area while continuing to drop the glass slide height. After complete contact is maintained for ~30 s, apply heat on the substrate to soften and lower the viscosity of the *Gelfilm* to facilitate dropping the 2D material onto the substrate. Lift and remove the glass slide quickly afterwards and inspect the substrate. This series of procedures is better understood through the animated slides shown in Figure 12.[43]

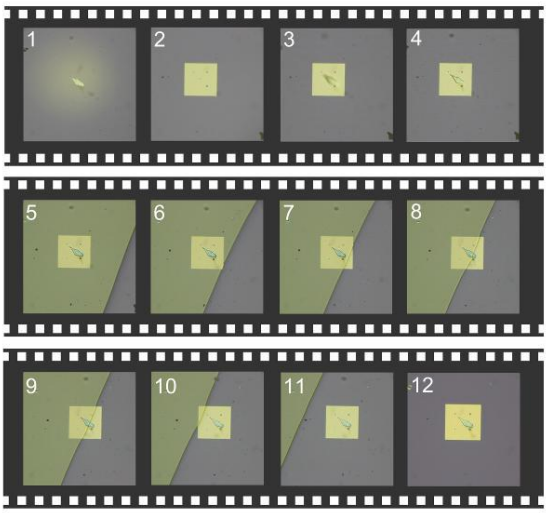


Figure 12: Frames of the real-time video acquired during the stamping of a single-layer MoS_2 onto a pre-patterned substrate. Yellow region is in contact without air gap.

3.3 CVD Layer Wet Transfer

The previous two sections demonstrate how to extract 2D material flakes from bulk crystal. 2D material could also be grown on specific substrates (such as CVD graphene on copper/nickel films) and requires "peeling off" to be transferred onto other substrates for further characterization or device fabrication. Taking single-layer graphene grown on copper foil as an example, the following wet transfer steps are typically applied. Note that the chemical (PMMA and copper etchant) may damage the grown layer's quality.

1. The graphene layers are on both sides of the copper foil. For detailed growth process, please refer to References 14 and 15. Graphene should be single layer and transparent. Spin PMMA on

top of graphene on one side (495A2, 3000 rpm for 30 s), usually the outer surface in CVD process (crossed section shown in Figure 13).

Figure 13: CVD graphene on copper with PMMA after step 1.

2. Prepare copper etchant ($FeCl_3$, type CE-100) in beaker 1 and DI water in beaker 2 and beaker 3.
3. Put a piece of PMMA/graphene/Cu/graphene foil (size ~ 1cm × 1cm, according to the size of the Au/Si substrate in this case) gently on the etchant surface. After ~2 min of floating, the back side graphene (not covered by PMMA) should turn into some material that looks like black ash due to the partial copper removal. Rinse the piece in beaker 2 with DI water.
4. Put the foil back into copper etchant and make it float on etchant. Repeat rinsing process in step 3 if more black graphene dust appears (crossed section shown in Figure 14).

Figure 14: CVD graphene on copper with PMMA after step 4. Graphene on one side is removed.

5. After ~10 min, copper should be almost completely etched away, leaving the PMMA/graphene membrane floating on the etchant. Use a SiO_2 wafer sample to carefully scoop it and pick it up (crossed section shown in Figure 15).

Figure 15: CVD graphene on substrate after transfer process described in step 5.

6. Put graphene/PMMA membrane into beaker 2 and rinse it with DI water.
7. Repeat this pick-up/rinse process (step 5, 6) in beaker 3.
8. After rinsing in beaker 3, pick up the membrane and try to make it flat on the device sample wafer. Nitrogen gun can be used with care to gently flatten the membrane.
9. Wait for 30 min for the water to evaporate.
10. Remove the PMMA by drenching the membrane/sample in acetone solution. Blow the sample dry after acetone is removed. Now the graphene layers are transferred onto SiO_2 wafer for further inspection (crossed section shown in Figure 16).

Figure 16: CVD graphene on substrate after PMMA removal described in step 10.

3.4 Identifying Transferred Material

After 2D material flakes are transferred onto acceptor substrates, it is necessary to confirm their shape, size, thickness, and contact with substrate to ensure that proposed structures would be appropriately fabricated. An optical microscope is the most accessible and low-cost tool for rough

inspection. Color contrast between the substrate and flakes transferred reveals the thickness. For atomic layers of 2D material, the color difference is barely visible. It generally holds that the thinner the layer, the lighter the contrast. For thick crystals among all the flakes transferred, their color ranged from green, to purple, to red, and to yellow, depending on specific material and thickness. An image process tool such as *ImageJ* could be used to numerically calculate the contrast between material body and substrate, providing a more reliable tool to determine material thickness.[39] Two example graphene optical images are discussed below in Figure 17.

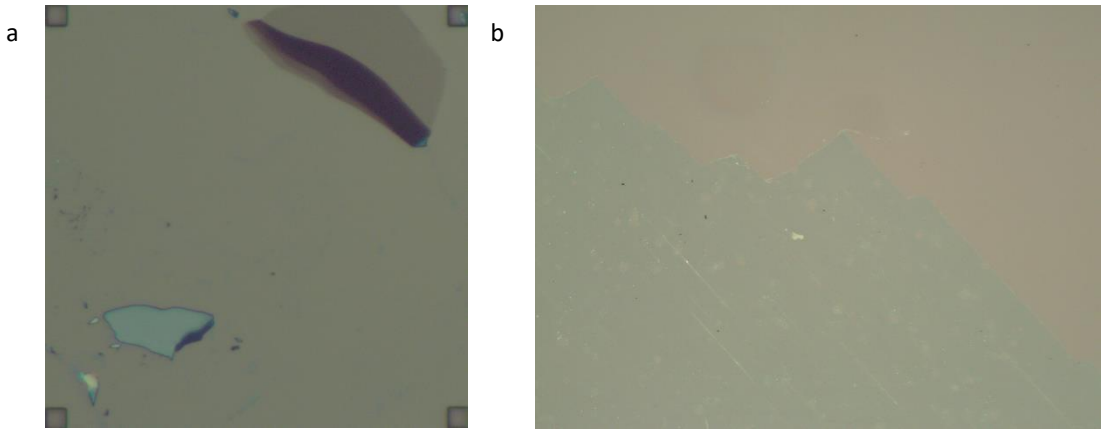


Figure 17: Mechanically exfoliated (upright corner in (a)) and wet-transferred CVD-grown (green area in (b)) single-layer graphene. Flake area with deeper color is multi-layer graphite (left). Strips on CVD-grown graphene are likely results from wet chemical etching and PMMA removal.

Raman spectroscopy and atomic-force microscopy (AFM) are widely used to determine the precise thickness of material. Specifically, the peak location and height of the Raman signal (with an example in Figure 18[22]) are signatures of the material since it reflects the unique vibration mode within the material and hence the interaction with incoming photons. Even for identical 2D material, samples with different thickness will slightly affect the peaks' relative location and height.[22, 44] On the other hand, AFM is the most intuitive and direct way to physically measure the target area's height with respect to substrate and is always used when a new 2D material is found in the field. Two-dimensional material has

typical thickness from 0.5 nm to 1 nm.[5, 18] Other identification methods include scanning electron microscopy (SEM), X-ray diffraction (XRD), etc., and are applied in special cases with different strengths and limitations.[45]

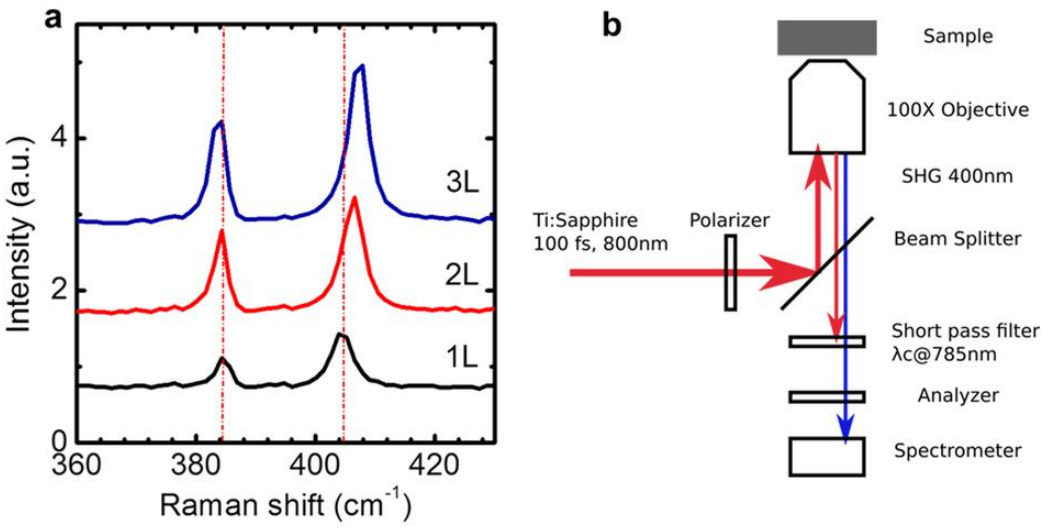


Figure 18: (a) Raman signals from different thickness of MoS_2 and (b) tool setup.

3.5 Patterning Structure with 2D Material

As in other traditional semiconductor devices, optical and/or e-beam lithography can be used to pattern the structure layer with corresponding etching or metal deposition/lift-off. For example, if we need to form specific dimension for the graphene channel in our FET or Hall-bar device, an AZ5214E photoresist strip by regular optical lithography could be used as a mask to protect the channel beneath it while oxygen plasma could etch away the excessive part from our transferred 2D material flake or CVD layer. With the help of alignment marks on the wafer substrate, we could also align the physical location of the 2D material on wafer with the mask designed by computer for e-beam lithography. Metal contacts are often designed this way prior to e-beam evaporation with lift-off due to the random position, size and shape of the 2D material flakes on the substrate.

Another common step involved in the construction of electronic devices is deposition of dielectrics. For 2D material devices, this could be done with a conventional dielectric growth method (atomic layer deposition of aluminum oxide/hafnium oxide, low pressure chemical vapor deposition of silicon nitride, etc.) or targeting transfer of 2D insulator. Some channel materials, such as black phosphorus, are sensitive to high temperature and special treatment or an alternative path needs to be considered.

With these basic concepts and the understanding of basic device fabrication techniques of 2D material, we are able to design devices with novel material or structure. In the following chapters, we will introduce black phosphorus back-gated FET and capacitors built from 2D materials using the methods described this chapter. We will also see how traditional device fabrication techniques could be integrated into 2D material device fabrication.

4. Example Device: Black Phosphorus Back-Gate Field-Effect Transistor

In this short chapter, we show a simple back-gated transistor which is fabricated using mechanical exfoliation method and its I-V curve (Figure 19). A relatively thin layer is located under the microscope (~10 nm, corresponding to ~20 layers). The source/drain contacts are defined by optical lithography with pre-registered patterns on the mask, and are deposited with an e-beam evaporator using gold target.

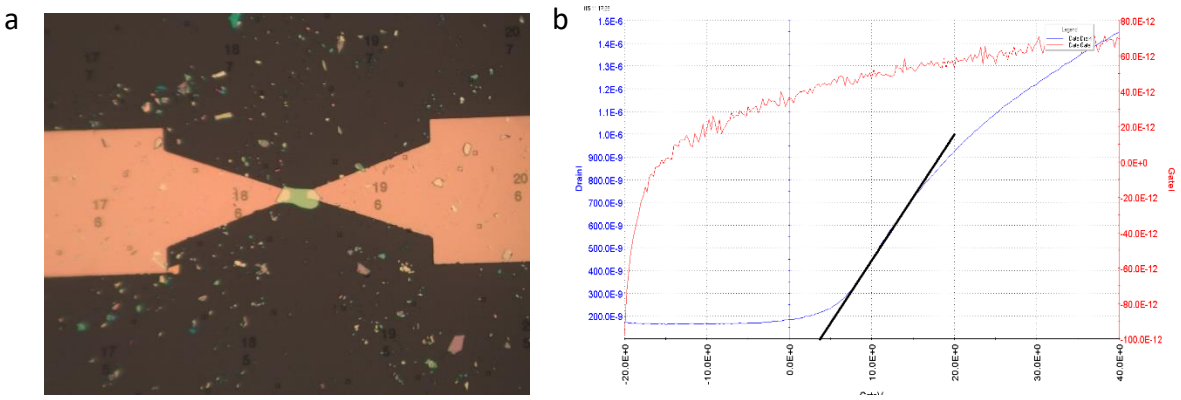


Figure 19: (a) Optical image of BP back-gated transistor fabricated. Gate voltage is applied on back side of the wafer with SiO_2 as dielectrics. (b) Id-Vg curve is measured at room temperature with V_{sd} = 0.3 V.

The I-V curve indicates the device is behaving as an n-type MOSFET. Using the simplified model for the I_d-V relationship in the MOSFET in triode region:[46]

$$I_d = \frac{W}{L}\mu C\left(V_g - V_t\right)V_{sd} \qquad (4.1)$$

where I_d is channel current, W and L are dimensions of the device, C is capacitance per unit area of the dielectric, μ is channel carrier mobility, V_g is back-gate voltage, V_t is threshold voltage and V_{sd} is voltage between source and drain. With the calculation of C, the slope in this region (estimated as slope of the black line in Figure 19) is then:

$$slope = \frac{W}{L}\mu C V_{sd} \tag{4.2}$$

$$C = \frac{\varepsilon_0 \varepsilon_r}{t} \tag{4.3}$$

With the microscope we estimate the dimension of the BP flake (length × width ~ 9 μm × 2 μm) and the relative dielectric constant (~3.9) [46] and thickness (90nm) for silicon dioxide. We calculated the carrier mobility of the channel to be ~9.84 $cm^2/(V{\cdot}s)$, which is smaller than the typical value ~100 $cm^2/(V{\cdot}s)$ reported in other work.[47] This may be due to the fact that our black phosphorus has been degraded in exposed air and the ohmic contacts formed.

5. Example Device: Black Phosphorus Capacitors on Quartz Wafers

This chapter reports the fabrication, measurements, and analysis of capacitors with black phosphorus (BP) as the semiconductor and hexagonal boron nitride (hBN)/aluminum oxide (Al_2O_3) as the dielectrics using mechanical exfoliation, dry transfer technique, and atomic layer deposition (ALD). We probed the intrinsic and extrinsic properties of BP using AC conductance and capacitance methods. By measuring the temperature and frequency dependence of capacitance and AC conductance of the BP capacitors, the band gap, doping concentration and interface trap density/time constant were extracted. This information is critical for designing and optimizing electronic devices such as transistors, TFETs and RTDs based on BP.

5.1 Experiments

The BP capacitors were fabricated on quartz substrates to eliminate the potential parasitic capacitance between the probe pads and substrates. An embedded metal electrode (30 nm Ti/ 20nm Au) was formed by optical lithography, e-beam metal evaporation and lift-off. The BP flakes were exfoliated from bulk crystal and stacked onto the bottom metal electrode using aligned dry transfer technique.[43] Two different gate dielectrics were formed in separated devices: hexagonal-boron nitride (hBN) and aluminum oxide. Our BN is exfoliated from bulk crystal, while Al_2O_3 was grown using atomic layer deposition at 200 ˚C.[48] Then the top electrodes were formed by lithography and metallization. The device structure of the BP capacitors is illustrated in Figure 20a.

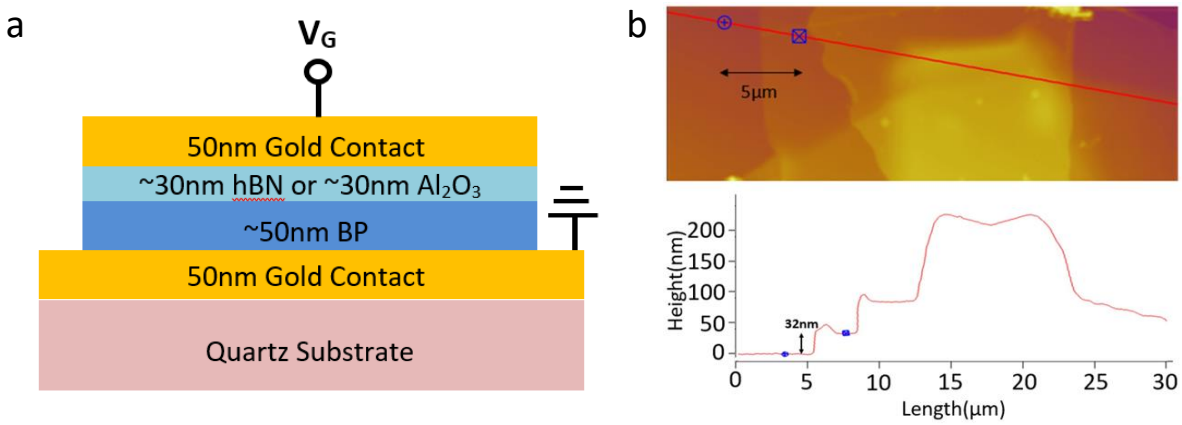


Figure 20: (a) Device structure. (b) AFM image of the hBN/BP MIS device focusing on the stack region. The red line scans across the step height of different materials. The two points indicate hBN thickness is ~32 nm. BP thickness is estimated to be ~50 nm from other AFM images.

5.2 Results and Discussion

The atomic force microscopic image and the step height profile for the BP/BN capacitors are shown in Figure 20b. The BP thickness is ~ 50 nm and hBN thickness is ~32 nm. For BP/Al_2O_3 capacitor, the Al_2O_3 thickness is ~ 30 nm by profilometer measured on the control structure. C-V measurements were performed in vacuum at frequency ranging from 10 kHz to 4 MHz and at temperatures ranging from 50 K to 300 K in a Lakeshore cryogenic probe station.

The frequency and temperature dependence of the capacitances in BN/BP capacitators were systematically studied by both experiments and modeling, with representative normalized CV curves shown in Figures 21 and 22. Notice that for both kinds of our devices the capacitances reach accumulation at negative gate voltage, indicating that BP is p-type doped in these sample. The maximum accumulation capacitance here should be only accounted for by insulator capacitance. Our calculated C_{ox} for hBN is 8.02×10^{-8} F/cm^2 and C_{ox} for Al_2O_3 ranges from 2.57×10^{-7} F/cm^2 to 2.82×10^{-7} F/cm^2. Relative permittivities calculated by $\epsilon_r = \frac{t\times C_{ox}}{A\epsilon_0}$ are 2.90 and 8.71 ~ 9.56 for hBN and Al_2O_3 respectively. These

values agree with previous reported work.[49, 50] We noticed the C_{ox} variation[51] with temperature, and we used a metal-insulator-metal structure on the same substrate with the Al_2O_3 device to record this change and for normalization. Since there is no intentional doping in the samples and the highly inert BN flake were mechanically stacked on BP at room temperature, this p-type doping is the natural doping in the original crystal. In Figure 21a, we can see that at a given temperature (300 K), as the frequency reduces, the C-V gradually changes from high-frequency-like behavior to low-frequency-like behavior. Here high-frequency-like C-V is defined as the C-V without a local minimum around the weak inversion region, while low-frequency-like C-V refers to the C-V with increased capacitance in strong inversion region.[52] This is because, as the measurement frequency reduces, the minority carriers have more time to respond to the ac signals. At a given frequency, as the temperature increases, the C-V will also gradually change from high-frequency-like to low-frequency-like behavior (Figure 21b) since more minority carriers will be generated thermally or excited from the traps as the temperature increases. The steepness of the curves at different temperatures could also be explained by the doping's ionization level dependence on temperature.[53]

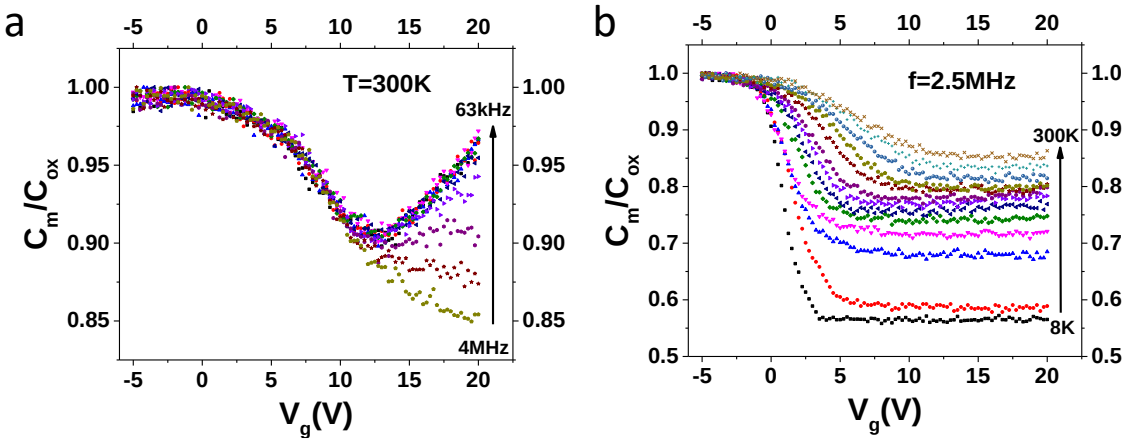


Figure 21: (a) hBN device C-V measured at different frequencies at 300 K. (b) hBN device C-V measured at 2.5 MHz at different temperatures.

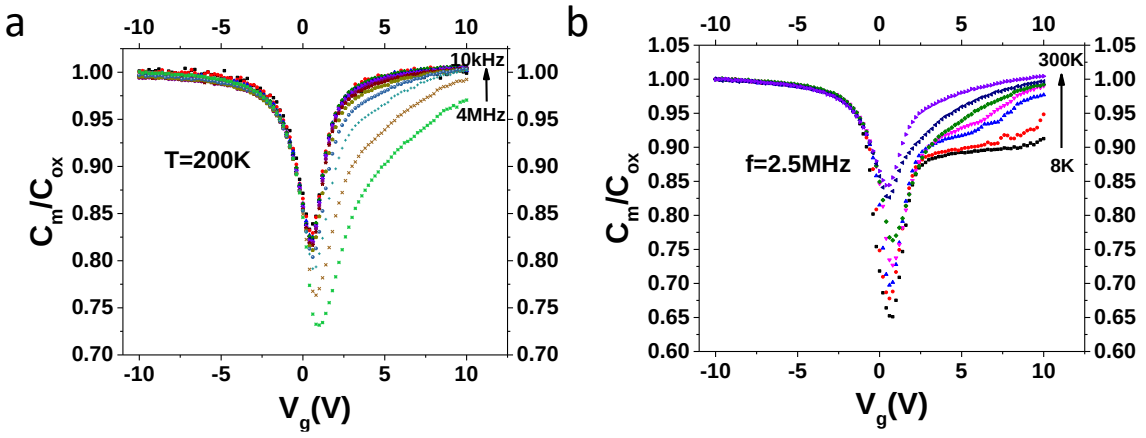


Figure 22: (a) Al_2O_3 device C-V at 200 K. (b) Al_2O_3 device C-V measured at 2.5 MHz at different temperatures.

Based on the above, transition frequency, f_T, is defined as the frequency where the C-V switched between high frequency and low frequency. Assuming the minority carrier response time (τ_R) is dominated by the trap assistant process, it can be shown that:[52]

$$\tau_R = \frac{1}{\sqrt{2}}\left(\frac{N_A}{n_i}\right)\tau_T\left(1-\frac{v_T}{u_B}\right)^{1/2} \tag{5.1}$$

$$f_T \propto \frac{1}{\tau_R} \tag{5.2}$$

where $u_B = q\phi_B/kT$ reflects the difference between the fermi level and intrinsic level, and V_T reflects difference between bulk trap level and bulk intrinsic level. τ_T represents averaged carrier lifetime and is weakly temperature dependent. Also:[46]

$$n_i = \sqrt{N_c N_v}\, e^{-\left(\frac{Eg}{2kT}\right)} \propto T^{3/2} e^{-\left(\frac{Eg}{2kT}\right)} \tag{5.3}$$

Starting from ~150 K, n_i is dominantly a strong function of the natural exponential term. In other words, f_T should follow exponential decay with 1/T. Figure 23 shows the plot of transition frequency as a function of 1000/T in log scale. From the slope of the curve, we extracted that the bandgap of the BP is 0.314 eV.

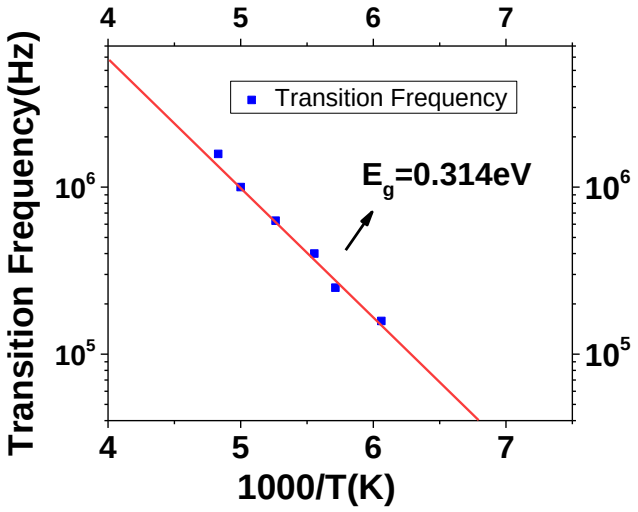


Figure 23: Temperature dependence of transition frequency (from 160 kHz to 1.6 MHz) device. The corresponding temperature ranges from 165 K to 210 K. The slope gives an estimated band gap ~0.314 eV.

We modeled the CV characteristics of the BN/BP capacitors using a simple electrostatic model. The charges in the BP can be expressed as:[46]

$$Q_s = -sign(\phi_s)\frac{\sqrt{2}kT\epsilon_s}{qL_D}\left[\left(e^{-q\boldsymbol{\phi_s}/kT} + \frac{q\phi_s}{kT} - 1\right) + \frac{n_0}{p_o}\left(e^{q\boldsymbol{\phi_s}/kT} - \frac{q\phi_s}{kT} - 1\right)\right]^{1/2} \quad (5.4)$$

where the Debye screening length $L_D = \sqrt{\frac{\epsilon_s kT}{q^2 p_o}}$, k is the Boltzmann constant, T is temperature, q is electron charge, p_0 is hole concentration at equilibrium, n_0 is electron concentration at equilibrium, ϵ_s is the permittivity of BP, and Φ_s is surface band bending. The low frequency capacitance of the BP can be

calculated by C_s=$\frac{dQ_s}{d\phi_s}$. The total capacitance of the capacitor is $C = (1/C_{ox} + 1/C_s)^{-1}$. The gate voltage is $V_G = V_{FB} + \phi_s - \frac{Q_s}{C_{ox}}$. For high frequency or low temperatures, where not all the minority carriers can respond to the AC signal, the effective inversion capacitance of the BP is model by $C_{inv\_eff} = C_{inv}/[1 + (\omega\tau)^2]$, where ω is the measurement frequency and τ is minority carrier response time.[52] The τ is different in two samples and it is made to change accordingly with different surface band bending. They are in the order of ~1E-6 s range for the BN sample and ~1E-7 s range for the Al_2O_3 sample. Some parameters used in simulation work are shown in Table 1.

Table 1. Parameters used in program fitting

Relative dielectric constant ε_r	6.1 for BP[54] 3 for hBN[49] 7.8 for Al_2O_3[50]
ε_0	8.85E-14 F/m
Relative effective mass in BP	m_{h_x}=0.09 m_{h_y}=0.81 m_{h_z}=0.36 m_{e_x}=0.09 m_{e_y}=1.16 m_{e_z}=0.17[55]
Planck constant h	6.626E-34 m^2•kg/s
Boltzmann constant k	1.38E-23 J/K
q	1.602E-19 C
m_0 mass of electron	9.11E-31 kg
V_{fb}	-8.8V for BN; -0.8V for Al_2O_3

The interface trap is also considered in the modeling. Assume the interface trap energy distribution has the "U" shape in the band gap similar to silicon.[56] The energy distribution of the interface trap can be expressed as $D_{it} = D_{it0}e^{\phi_s/\phi_{s0}}$, where D_{it0} is the interface trap density at the mid-gap and ϕ_{s0} is a characteristic potential which describes the slope of D_{it} near the band edges. The

voltage stretch-out caused by the interface traps is $\Delta V_G = \frac{q\int_{E_i}^{E_F} D_{it}(\phi_s)dE}{C_{ox}}$, where E_i is the intrinsic energy level and E_i is the Fermi level at the BP/dielectric interface. The additional capacitance induced by the interface traps at low frequencies is $C_{it} = qD_{it}$ and at high frequencies or low temperatures is $C_{it\_eff} = C_{it}/[1 + (\omega\tau_{it})^2]$, where τ_{it} is the interface trap time constant. Figure 24a shows the modeled C-Vs and experimental data at various frequencies. For clarity only three frequencies and temperature are illustrated here. We can see that the modeling curves and the experimental results agree very well. From those modelings, we can extract that the bandgap of the BP is 0.37 eV and doping concentration is 3×10^{18} cm^{-3}. The thickness of the BN is 32 nm. This is the first report on the doping concentration measurement on BP, which will be important for future device designs based on BP. The bandgap extraction using C-V technique will also be a very useful tool for BP, since the band gaps of bulk or thick BP flakes are very small, typically outside the measurement window of photoluminescence and absorption spectrometry. Determining the bandgap electrically can overcome this limit and can be carried out in-situ on fabricated electronic devices.

In addition to BN, high-k dielectrics such as Al_2O_3 and HfO_2 are also frequently used as gate dielectrics for 2D materials. Figure 22 shows the CVs of the BP/Al_2O_3 capacitors at various frequencies and temperatures. One striking difference between CVs of BP/Al_2O_3 and BP/BN capacitors is that the C-Vs in BP/Al_2O_3 are much more ambipolar. This indicates that BP is much less p-type doped in BP/Al_2O_3 capacitors, which could due to the n-type counter-doping induced by the Al_2O_3 deposited at elevated temperatures (200 ˚C) in the ALD tool. We modeled the BP/Al_2O_3 C-Vs, shown in Figure 24b, at various frequencies and extracted the bandgap of 0.35 eV and doping concentration of 1.8×10^{18} cm^{-3}. Thickness of the Al_2O_3 is 30 nm. The bandgap of BP extracted from the BP/Al_2O_3 sample is consistent with that of the BP/BN sample. The doping concentration in the BP/Al_2O_3 sample, however, is much lower, which explains the ambipolar behavior of the CVs in BP/Al_2O_3 capacitors.

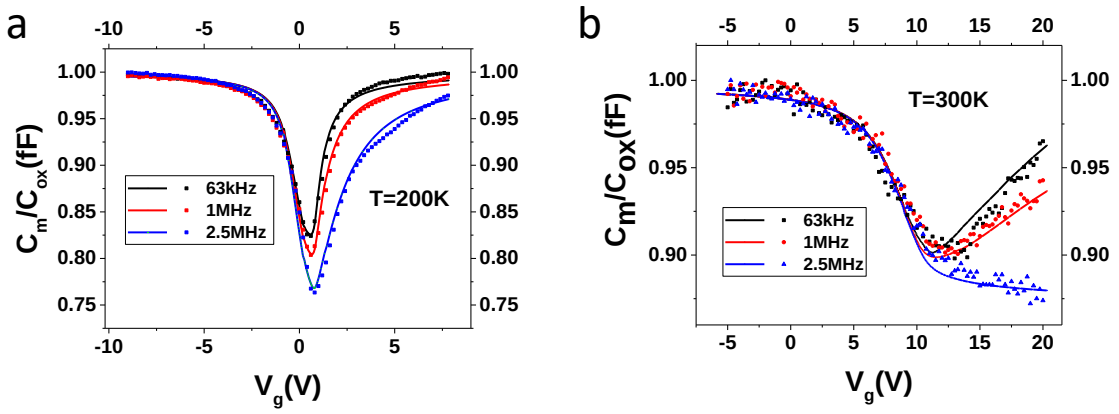


Figure 24: (a) Representative fitting C-V data vs. experimental C-V data for Al_2O_3 device. (b) Representative fitting C-V data vs. experimental C-V data for hBN device. (Lines: fitting; Dots: experimental.)

For BP/Al_2O_3 capacitors, the frequency dispersion at minimum capacitance is much larger than for BP/BN samples, indicating the potentially higher interface traps.[57] To quantify the amount of interface traps, we measured the AC conductance and capacitance of the BP/Al_2O_3 capacitors at various temperatures and frequencies, shown in Figure 25a. The equivalent circuit is illustrated in Figure 25b. The parallel conductance G_p can be extracted by using the following equation by circuit conversion:[52]

$$\frac{G_p}{\omega} = \frac{\omega G_m {C_{ox}}^2}{{G_m}^2 + \omega^2 (C_{ox} - C_m)^2} \tag{5.5}$$

G_m and C_m here are measurement data with parallel area G and C subtracted. The interface trap density and time constant can then be evaluated by data fitting or derivation as following [52]:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln[1 + (\omega\tau_{it})]^2 \quad (5.6)$$

$$D_{it} = \frac{2.5}{e}(\frac{G_p}{\omega})_{peak} \quad (5.7)$$

$$\frac{G_p}{\omega} = \frac{1.98}{2\pi f_0} \quad (5.8)$$

Here, $(G_p/\omega)_{peak}$ is the maximum G_p/ω value and f_0 is the frequency at which this maximum G_p/ω is obtained. The extracted D_{it} and τ_{it} as functions of gate voltages at various temperatures are shown in Figure 25c and 25d. We found that as the gate voltage decreases, i.e. energy level is closer to valence band edge, the interface trap density increases and the time constant reduces. This again is similar to the interface trap distribution in silicon, which is reported to have a "U" shape trap density distribution in the bandgap.[56] As the energy level approaches the band edge, the trap levels more easily exchange carriers with the valence band, which gives a shorter time constant. As the temperature increases, the interface traps have higher capture and emission rates, which will result in shorter interface trap time constant.

Compared to the BP/Al_2O_3 capacitor, the BP/hBN sample has non-obvious ac conductance signal peaks. We estimate its D_{it} values are approximately one tenth those of the BP/Al_2O_3 sample in depletion region while its τ_{it} values are in the ~10^{-5} s scale. Comparing Al_2O_3 and BP, the interface tap densities in the BN/BP capacitors are much lower than those in BP/Al_2O_3 capacitors, indicating superior quality of the single-crystal BN. However, Al_2O_3 has the advantage of wafer scale deposition while BN flake thickness/size is hard to control. For arrays of electronic devices, high-k dielectrics will still be necessary. This C-V characterization technique will be a useful method to monitor the process, quantify the trap densities, and provide direction on process optimizations. For tunneling devices, such as TFETs and RTDs, the interface trap density is vital. The trap density will directly determine the subthreshold slope

of the TFET. In an ideal device without interface traps, the band-to-band tunneling in TFET can enable super-steep subthreshold slope. In a real device with interface traps, however, the subthreshold slope is highly influenced by the number of traps. The key to achieving super-steep subthreshold swing in TFET is to minimize interface traps. The interface traps will directly determine the valley current and peak-to-valley current. In these electronic devices, this AC conductance and capacitance characterization technique will be critically important.

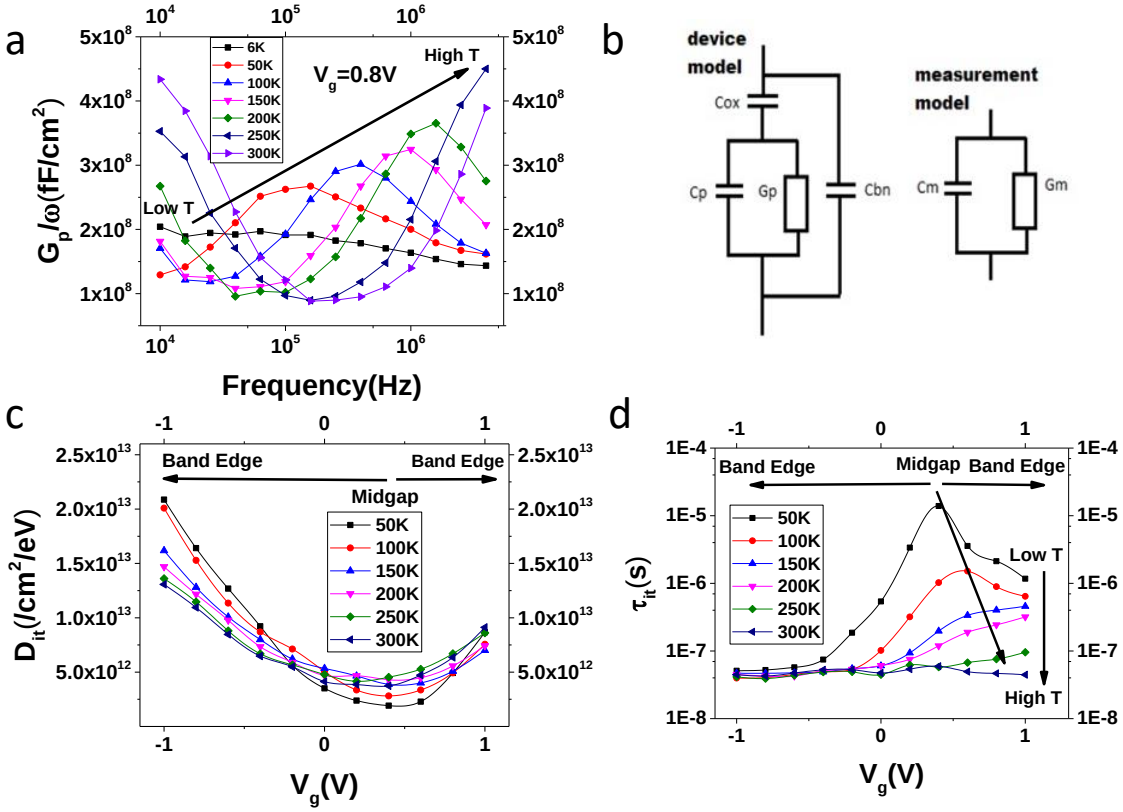


Figure 25: (a) Device physical model and measurement model used in probe station. C_{ox} refers to the capacitance of hBN from with BP beneath it and C_{bn} refers to the capacitance of hBN without BP beneath it, which is subtracted from our CVs in this work. (b) A typical Al_2O_3 device G_p/ω plot at 0.8 V gate bias (depletion region). (c) Extracted D_{it} at different bias and temperature. D_{it} increases as its energy level approaches band edge due to easier carrier transfer. (d) Extracted τ_{it} at different bias and temperature. τ_{it} decreases as temperature increases due to higher thermal energy. As energy level approaches band edge, lifetime is shortened for facilitated carrier filling/emission.

5.3 Summary

In this chapter, we have systematically studied the intrinsic and extrinsic properties of BP using ac conductance and capacitance methods. From the temperature and frequency dependence CV in BP/BN capacitors, we extracted that the bandgap of BP is 0.31 eV and doping of ~3 × 10^{18} cm^{-3}. From the ac conductance of the BP/Al_2O_3 and BP/BN capacitors, we extracted the interface trap density and time constant. We found that the interface trap density in Al_2O_3 is about 10 times that in BP/BN capacitors, indicating the superior quality of the single-crystal BN. In addition, we found that the interface trap density increases and the time constant is shorter as the trap level is closer to the valence band.

6. Conclusion and Future Work

In this work, we introduced the discovery of 2D material and its unique potential for electronic devices. Several important 2D materials under study nowadays were reviewed with their physical/chemical properties, device application, and growth method. Then we detailedly demonstrated the basic method to extract 2D material thin layers from bulk crystal or CVD substrate and transfer them to desired locations for further study of device structure. Commonly used tools to identify 2D materials and lab techniques to build devices were discussed.

Based on these, we successfully demonstrated current flow through the BP channel with back-gate tuning. We have also systematically studied the intrinsic and extrinsic properties of BP experimentally and simulated the C-V characteristics of the BP capacitors using a simple electrostatic model to quantify BP's band gap and doping. From the temperature and frequency dependence of the C-Vs in BP/BN capacitors, we determined the bandgap of BP. From the AC conductance of the BP/Al_2O_3 and BP/BN capacitors, we calculated the interface trap density and time constant and made comparison analysis. Finally, we concluded that the Al_2O_3 deposited by ALD introduces n-type doping to the black phosphorus.

In the future, we will continue studying the properties of the BP with various numbers of atomic layers and under varying magnetic fields. In addition, we will combine BP with ferroelectric materials and create novel electronic and optoelectronic devices, such as ferroelectric memories, tunneling field effect transistor, and photodetectors. These devices will have broad applications in computing, communications, and biomedicine.

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